ULTRA-THIN SILICON COMPLAINT LAYERS FOR INFRARED MATERIALS

August 1998

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ABSTRACT

A simple method for the manufacture of an ultra-thin (<5nm) silicon layer that is bonded to a handle substrate for compliant substrate applications has been demonstrated. Compliant substrates have potential benefit for reducing defects in epitaxial materials grown on a large lattice mismatched substrates, including the growth of CdTe and HgCdTe on silicon substrates. In addition, an approach to fabricate a HgCdTe detectors directly over CMOS readout circuitry by epitaxially growing HgCdTe on a thin (211) silicon layer that is wafer bonded to the CMOS wafer is described.

1.0 INTRODUCTION

While the material quality of HgCdTe grown on silicon is sufficient for mid-wave infrared detectors, additional improvement in material quality is desired for long wavelength IRFPAs [1]. One candidate approach to improving the quality of long wavelength HgCdTe material grown on silicon is the compliant substrate approach {2, 3, 4].

One of the most critically important technologies for compliant or universal substrates is a reliable, manufacturable technique to fabricate the ultra-thin semiconductor layers required for compliant substrates [2, 4]. In the past, ultra-thin semiconductor layers have been produced by successive oxidation and oxide etching of SOI wafers [5] and, in the case of GaAs, by epitaxial lift-off [6] and etch stop [3] techniques. These techniques suffer from non-uniformities in the etching of semiconductor layers which makes the processes unsuitable for producing very thin semiconductor layers in a manufacturing environment.

In this work, an approach is adopted that combines two existing SOI substrate fabrication techniques and effectively eliminates the primary disadvantage of each method. The bond-and-etch back technique for fabricating SOI substrates (BESOI) has been combined with the hydrogen implantation and separation technique (also called Smart-Cut) [7]. The BESOI process has been shown to produce highly uniform thin Si (˜200 nm) layers by incorporating an epitaxial $Si_x Ge_{1-x}$ etch stop layer into the host substrate prior to wafer bonding [8, 9]. The disadvantage of the BESOI approach is that the entire host substrate must be removed by a laborious sequence of grinding, polishing, and etching. In addition, overall thickness uniformity during the substrate thinning process must be critically maintained since the etch selectivity of Si over SiGe is limited (<100). The H implantation and separation process also utilizes wafer bonding, but in this case a heavy dose of implanted H together with subsequent annealing produces H exfoliation that releases the host substrate to generate the SOI structure. The surface following exfoliation has a

REPORT DOCUMENTATION PAGE

Form Approved OMB No. 0704-0188

1. REPORT DATE (DD-MM-YYYY)	2. REPORT TYPE	3. DATES COVERED (FROM - TO)
01-08-1998	Conference Proceedings	xx-xx-1998 to xx-xx-1998

4. TITLE AND SUBTITLE
Ultra-Thin Silicon Complaint Layers for Infrared Materials
Unclassified

5a. CONTRACT NUMBER
5b. GRANT NUMBER
5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)
Kub, Fritz J. ;
Hobart, Karl D. ;

5d. PROJECT NUMBER
5e. TASK NUMBER
5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME AND ADDRESS
Naval Research Laboratory
Washington, DC20375

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME AND ADDRESS
Director, CECOM RDEC
Night Vision and electronic Sensors Directorate, Security Team
10221 Burbeck Road
Ft. Belvoir, VA22060-5806

10. SPONSOR/MONITOR'S ACRONYM(S)
11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT
APUBLIC RELEASE
,

13. SUPPLEMENTARY NOTES
See Also ADM201041, 1998 IRIS Proceedings on CD-ROM.

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15. SUBJECT TERMS

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19. NAME OF RESPONSIBLE PERSON
			Public Release	8	Fenster, Lynn lfenster@dtic.mil
a. REPORT Unclassified	b. ABSTRACT Unclassified	c. THIS PAGE Unclassified			19b. TELEPHONE NUMBER International Area Code Area Code Telephone Number 703767-9007 DSN 427-9007

microroughness of about 8 nm [7] and must be given a slight chemomechanical polish to produce a prime surface. This step degrades the Si layer thickness uniformity and makes the process unsuitable for producing very thin Si films. The process presented here avoids the above stated disadvantages and, as shown below, is a simple method for producing uniform SOI wafers with Si thicknesses less than 10 nm.

2.0 ULTRA-THIN SILICON FABRICATION METHOD

The approach used to fabricate the ultra-thin silicon compliant layer is shown in Fig. 1. 100mm diameter, 10 ohm-cm, n-type, (100) orientation substrate were thermally oxidized in dry O_2 to produce 120nm of SiO_2 for the "handle" wafer fabrication. On a similar starting substrate, Si and Si_xGe_{1-x} films were epitaxially grow to form the "host" substrate. The nominal layer specifications were a 20nm Si buffer, followed by 30nm of $Si_{0.7}$ $Ge_{0.3}$ and 4nm of Si. All layers were B-doped to $\approx 10^{15} cm^{-3}$.

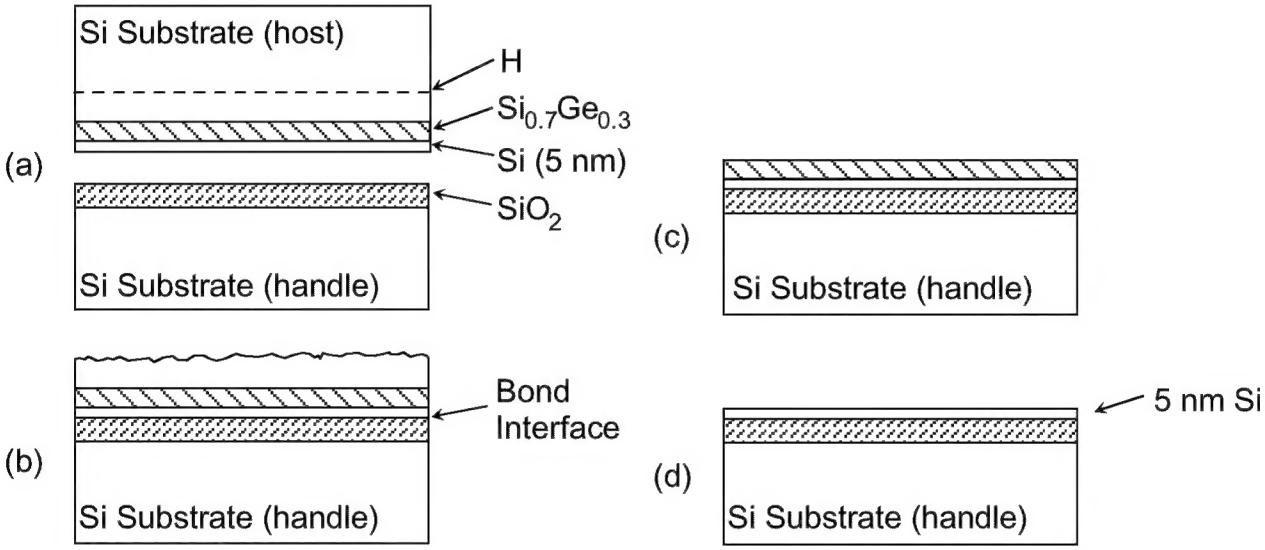

Figure 1. Ultra-thin SOI fabrication process
a Preparation of handle and host wafers prior to bonding
b Bonded wafer pair shown after separation of host substrate
c SOI structure prior to removing SiGe etch stop
d Ultra-thin SOI after removal of SiGe etch stop

The host substrates were implanted at room temperature with H_2+ with an ion energy of 180KeV and a dose of $4.5x10^{16} cm^{-2}$ (see Fig. 1a). Handle and host substrates were rendered hydrophilic by $NH_4OH:H_2O_2:H_2O::1:1:4$ and $HCL:H_2O_2:H_2O::1:1:4$ cleaning procedures. After a final rinse in de-ionized water, the wafers were spun dry. Wafer bonding was performed in a class 100 laminar flow bench using a custom designed jig to align the major wafer flats. Infrared transmission imaging showed the existence of several macorvoids near the wafer edge; otherwise the bonded pair was void-free. The wafer pair was annealed at 250°C for 4 hours to improve the bond strength. To separate the host substrate from the etch stop layer and handle wafer, the wafer pair was heated to 550°C for 10min in N_2 (Fig. 1b). Separation of the host substrate left ≈800nm of Si (including the SiGe etch stop and Si capping layer) on the SiO_2 film with a mean surface

roughness of ≈5-7nm, as measured by stylus profilometry. Film separation was successful over the entire 100mm wafer.

Nomarski microscopy revealed a textured surface resulting from the exfoliation process. No microvoids were observed in the separated film. Aqueous KOH (10% by weight) was then used to etch the Si and stop at the SiGe (Fig. 1c). The etch rate for Si at room temperature was found to be ≈30 nm/min and the etch selectivity to $Si_{0.7}$ $Ge_{0.3}$ was found to be ≈20. Following the Si etch Nomarski microscopy revealed no detectable surface roughness. The films were specular and extremely uniform to the eye. Since the etch rate of SiO_2 was negligible in KOH, remaining film thickness was measurable by stylus profilometry across the macrovoids near the wafer edge. The film thickness (Si + SiGe) was found to be 36nm. X-ray photoelectron spectroscopy (XPS) indicated that the actual etch stop composition was closer to $Si_{0.68}$ $Ge0_{.32}$. The SiGe layer was then selectively removed in a solution of $HF:H_2O_2:CH_3COOH$::1:2:3 [10]. The etch rate of $Si_{0.7}$ $Ge_{0.3}$ was found to be ≈100 nm/min at room temperature and the etch selectivity to Si was nearly 1000. Examination by Nomarski microscopy revealed no detectable surface features (other than the low density of microvoids) and the film appeared specular and uniform to the eye.

The ultra-thin SOI films were further characterized by XPS and high-resolution cross-sectional transmission electron microscopy (HRXTEM). The Si film thickness was estimated with XPS by measuring the attenuation of Si 2p core level electrons from the buried SiO_2. This peak is unambiguously identified since the binding energy is chemically shifted by +4.5 eV with respect to Si 2p electrons in bulk Si. From the known inelastic mean free path of Si 2p electrons in Si (2.1 nm) and the measured attenuation of the signal (92.4%), the Si thickness was estimated to be 5.2+/-0.5 nm. Ge 2p electrons were also detected with an intensity equivalent to that produced by a 5.0 nm thick $Si_{0.98}$ $Ge_{0.02}$ alloy with uniform Ge concentration. The actual Ge profile was not determined but its existence is possibly the result of surface segregation during heteroepitaxial growth. HRXTEM was performed on the as-fabricated ultra-thin SOI structure. A micrograph is shown in Fig. 2. From TEM it was determined that the Si thickness was closer to 4.0 nm and was uniform to within 20% over the sample studied. An AFM measurement over a 4μm x 4μm area obtained a RMS roughness of 0.159nm and a mean roughness of 0.111nm.

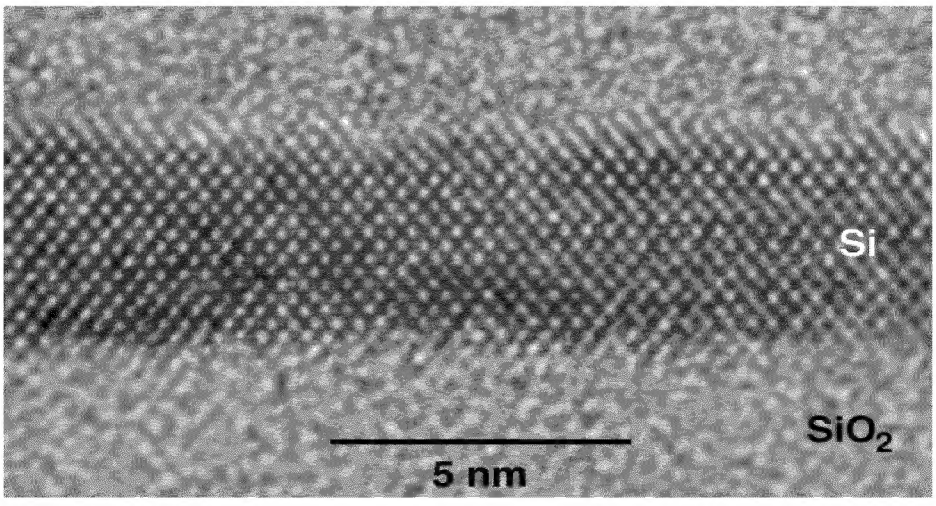

Figure 2. High resolution cross-sectional transmission electron micrograph of ultra-thin (≈4nm) silicon layer of SOI wafer.

3.0 APPROACH FOR HgCdTe DETECTOR OVER CMOS

A technology for implementing HgCdTe material directly over CMOS circuitry is potentially of interest as a lower cost method of producing infrared focal plane arrays. One approach to achieve HgCdTe growth over CMOS circuitry is to chemical mechanical polish (CMP) the CVD oxide layer that covers the CMOS circuitry, form a thin (211) silicon layer on the planarized oxide layer by direct wafer bonding as described below, and epitaxially grow an appropriate II-VI buffer layer on the (211) silicon layer. The thin (211) silicon layer can be formed using the hydrogen layer splitting and SiGe etch stop approach described above [11], however, for the case that a compliant layer is not required, hydrogen implant layer splitting followed by a polishing operation [6] is a possible approach to form silicon layers with a thickness of 100nm to 300nm. The typical anneal temperature required to cause the hydrogen gas to expand to cause the splitting to occur in silicon is typically in the range of 400°C to 500°C [7]. Another approach is to bond an SOI wafer to the CMOS wafer and use the SOI oxide layer as etch stop layer .

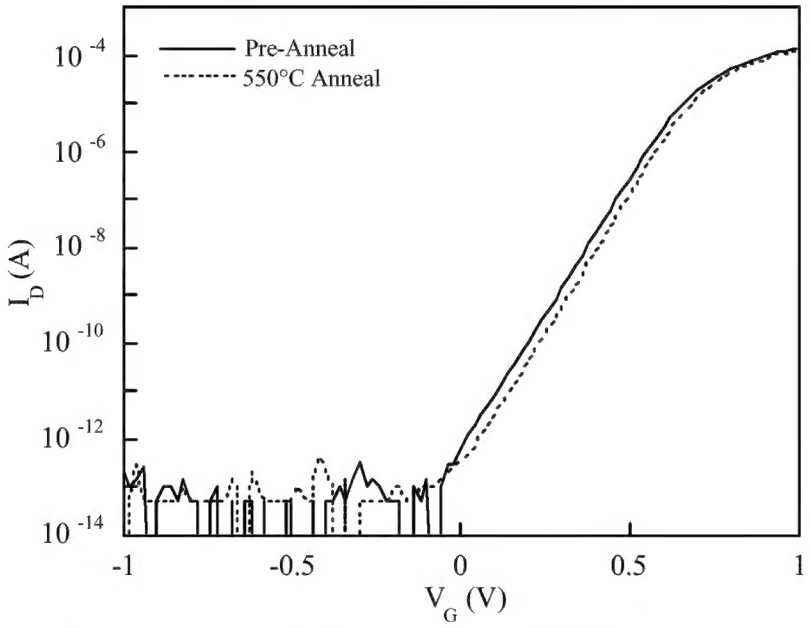

Figure 3. Subthreshold characteristics for N-channel MOSFET for pre and post 550°C, 1 min. anneal produced using 0.5μm CMOS technology from HP. W/L= 25μm/1μm, VD=100mV.

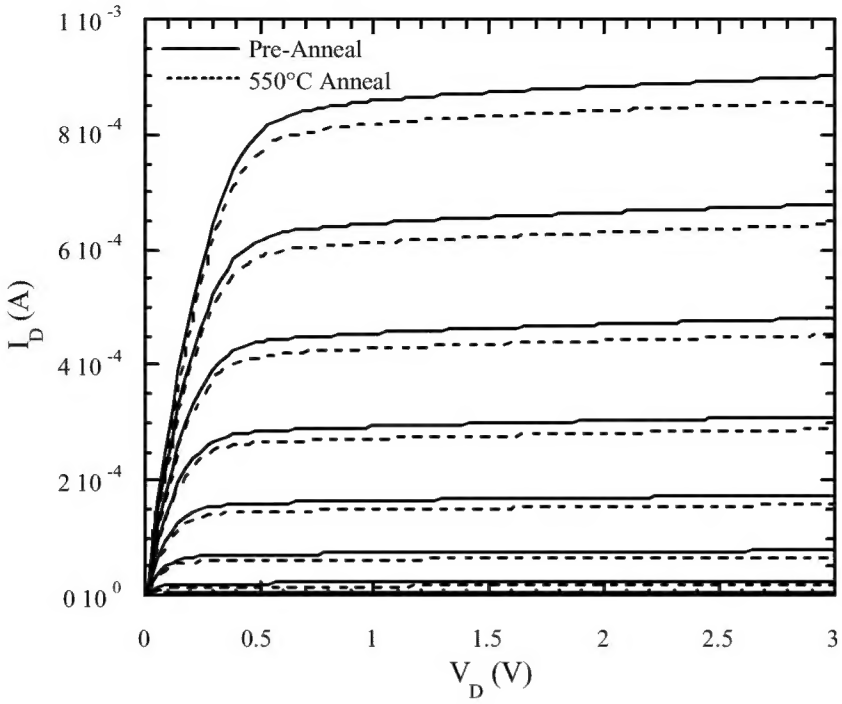

Figure 4. I-V characteristics for N-channel MOSFET for pre and post 550°C, 1 min. anneal produced using 0.5μm CMOS technology from HP. W/L= 25μm/1μm, V_G = 0.5V-1.3V, 100mV steps.

The critical issue for growing HgCdTe directly over top of CMOS circuitry is the ability of the CMOS circuits to withstand the temperature cycles involved in the growth of HgCdTe and CdTe layers on (211) silicon. Modern CMOS technologies are fabricated using a barrier metal layer (tungsten) between the aluminum interconnects and the silicide material that contacts the silicon junction. With the use of barrier metals, modern VLSI technologies can withstand temperatures of 500°C for extended times and may be able to withstand 550°C or higher temperatures for short times. The MBE growth of HgCdTe is typically performed at temperatures of approximately 180°C and the growth temperature for CdTe is typically 380°C [1].

A critical issue for the growth of epitaxial materials on a silicon surface is removal of the native oxide prior to epitaxial growth. One of the most common methods of preparing an oxide free silicon surface in a UHV growth system is to use the technique of hydrogen terminating the silicon surface [12], and then flashing off the hydrogen by a short temperature cycle in UHV. Typical temperatures at which hydrogen desorps are in the vicinity of 550°C. Thus, one option for the growth of II-VI material on a thin silicon layer directly over CMOS circuit is hydrogen terminate the silicon surface, desorp the hydrogen using a temperature cycle in the range of 550°C, and epitaxially grow the II-VI material. The feasibility of CMOS circuitry being able to withstand a 1 minute, 550C anneal was investigated by annealing transistors produced using the 0.5μm CMOS technology from HP obtained through MOSIS program from Information Science Institute. Figure 4 shows the subthreshold characteristic and Figure 5 shows the current-voltage characteristics n-channel MOSFET with W/L of 25μm/1μm produced using the 0.5μm CMOS technology. The subthreshold characteristics show no increase in junction leakage for the 550°C,

1 minute anneal, however, there is a slight change in the I-V characteristics after the 550°C anneal. The reason for the change in I-V characteristics has not been identified. All transistor measured (approximately 10) function normally after the anneal. The p-channel MOSFETs also functioned normally after the 550°C, 1 minute anneal. The measurements are encouraging for the possibility of growing HgCdTe directly over CMOS circuitry using 550°C anneal to desorb hydrogen from a hydrogen terminated surface.

A second option for growing HgCdTe material on a silicon layer directly over CMOS circuitry without exposing the CMOS circuitry to temperature > 400°C is to hydrogen terminate the silicon surface, however, only heat the silicon surface to a sufficient temperature to remove water vapor, hydrocarbons, and dihydrides, leaving the monohydride hydrogen on the surface during epitaxial growth. Eaglesham, et. al., [13] have demonstrated the MBE growth of silicon with a maximum cleaning temperature of 370°C. More complicated approaches of UV or excimer laser illumination in a UHV system are also possibilities for low temperature removal of hydrogen from the surface prior to epitaxial growth.

Several possible photodiode configurations are well to the case of HgCdTe directly over CMOS circuitry. The front side illuminated Vertically Integrated Photodiode (VIP™) [14] is one possible configuration. A possible alternate detector design for an HgCdTe PN diode over CMOS circuitry is shown in Figure 5. Key issues for the alternate proposed detector design are the method of etching the via in HgCdTe/CdTe, low temperature conformal oxide deposition for the oxide spacer, RIE etch of the oxide spacer, and plating of thick metal in the via.

4.0 SUMMARY

In conclusion, ultra-thin Si (<5nm) SOI has been fabricated, for the first time, by combining the BESOI and film separation by H-implantation techniques. This combined approach effectively eliminates the drawbacks associated with the individual processes and is capable of producing extremely thin SOI films with excellent thickness uniformity and low surface roughness. The key issues and approaches for forming a thin single-crystal silicon layer over top of CMOS circuitry and then epitaxially growing II-VI material on the thin silicon layer to implement HgCdTe infrared detectors on CMOS were discussed.

Acknowledgments

Work was supported by the Office of Naval Research. We would like to express our appreciation for fruitful discussion with John Jensen, Terry DeLyon, and Jim Waterman.

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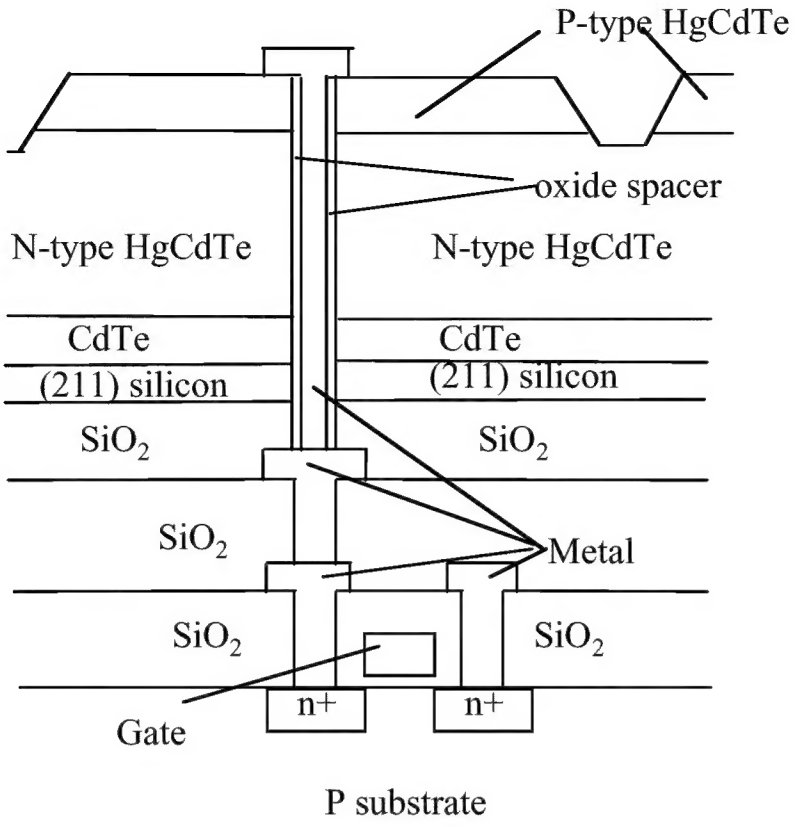

Figure 5. Possible detector design for an HgCdTe PN diode over CMOS circuitry.